The importance of fully-integrated CMOS: Cost-Effective Integrated DC-DC Converters

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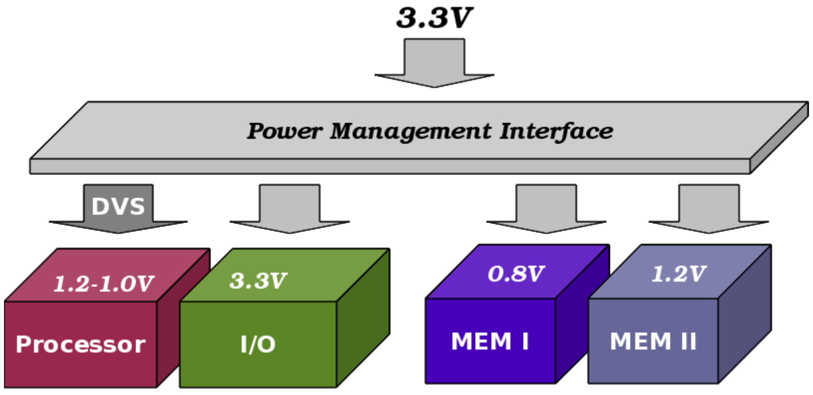
Overview

- **Introduction**
- DC-DC converters in CMOS
  - Passives
  - Active devices
  - Control
- Inductive
  - Converter Topologies
  - Converter Components
  - Control Systems
- Capacitive
  - Low Power
  - High Power
  - Exotic Cheap Technologies -> Organic DC-DC Converter

Introduction: Why & What?

- Bridge the Voltage Gap
  - Battery Voltage vs Supply Voltage
  - POL Converter close to load

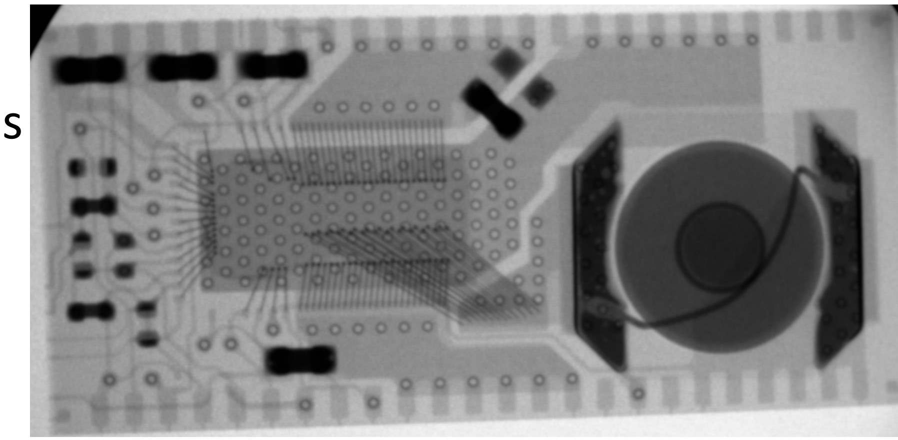


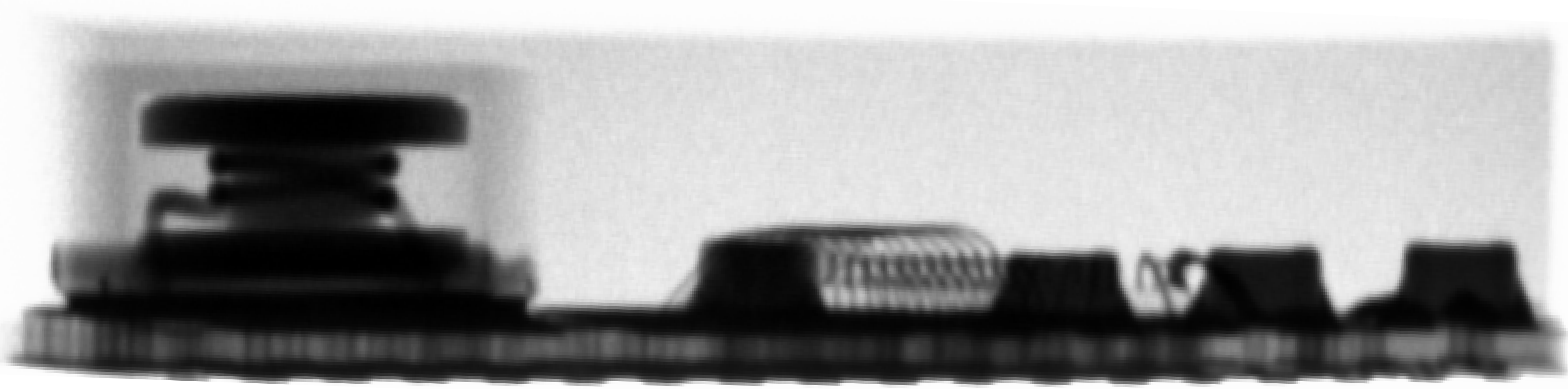
- Enables
  - Multiple Voltage Domains
  - Voltage Scaling (AVS &DVS)

Need for DC-DC converters as basic building blocks

How DC-DC: SoC vs SiP

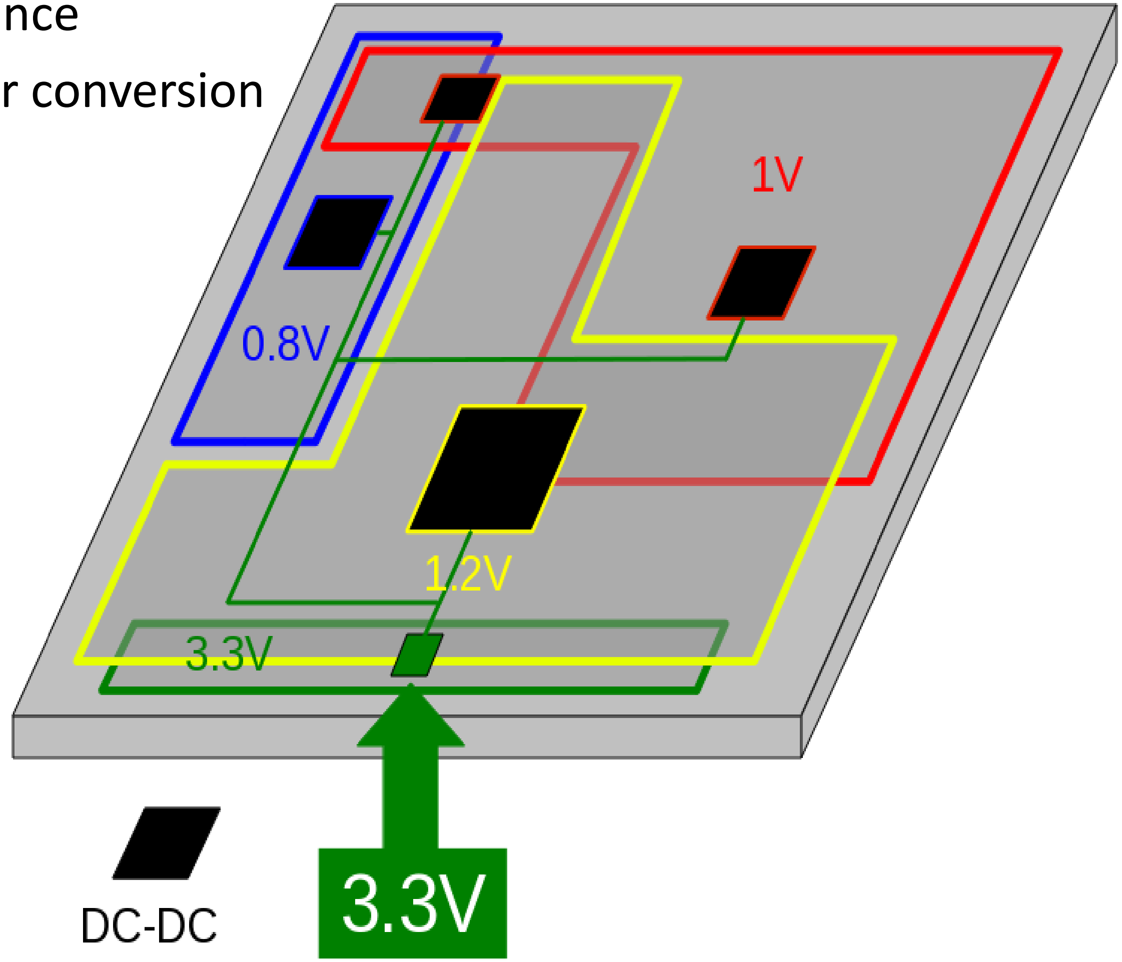
- PowerSiP
  - Bondwire interconnect to passives
  - # components vs footprint
  - Larger passives
  - Cost does not scale fully with production volume due to PCB and component cost





How DC-DC: SoC vs SiP

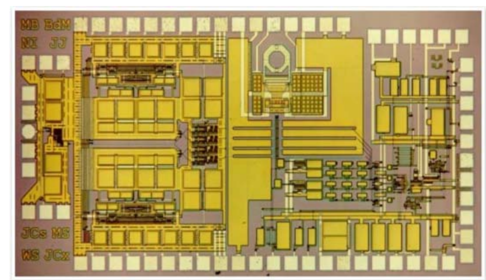
- PowerSoC
  - Very low supply impedance
  - Full decentralized power conversion (powergrid on chip)
  - Many voltage domains
  - Scalable
  - Small footprint
  - Cost scales with production volume



A Trend: (r)evolution

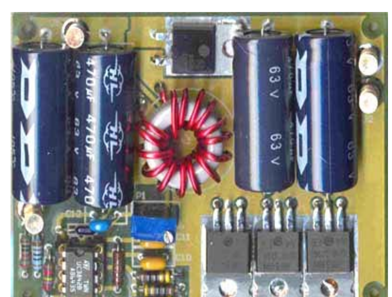
- Integration Paradigm
  - In RF-CMOS it brought us portable, low cost and versatile applications

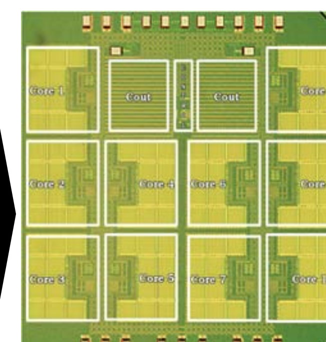
  → A true technology revolution



- Monolithic Integration of power electronics?
  - Even more compact utilities
  - Less energy losses
  - Longer Battery Lifetime (EEF)

  → POWER-CMOS will complete the evolution that started with RF-CMOS





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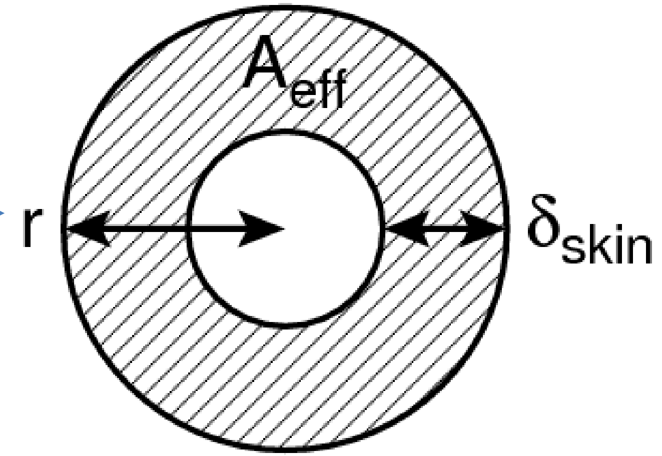
DC-DC in CMOS: Passives

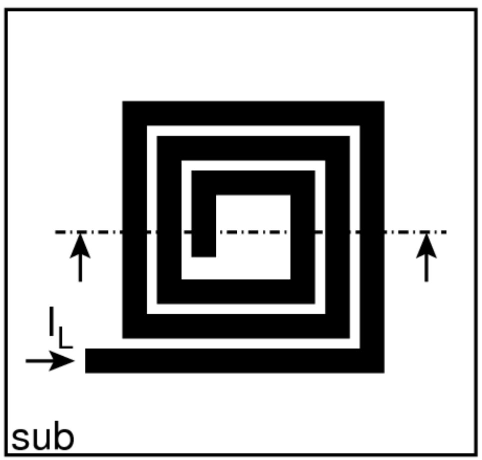
- Inductors
  - Integration awareness of inductors
  - Bond wire inductor
  - Metal track inductor

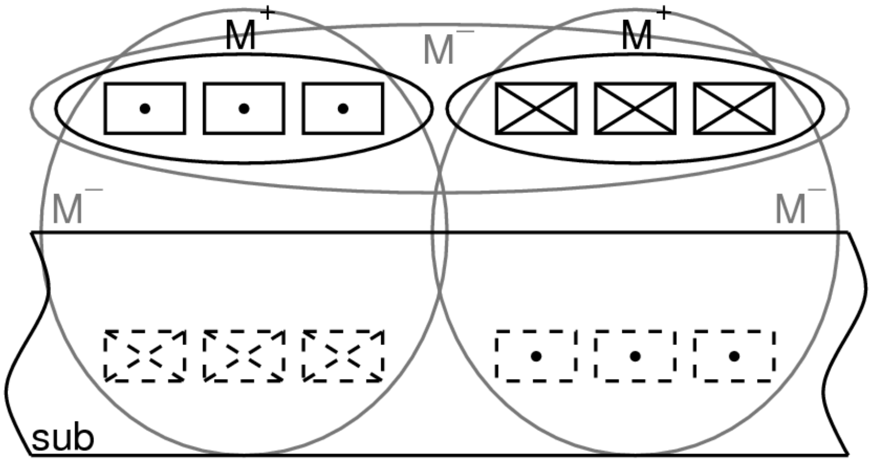
Passives in CMOS

Inductors on-chip:

- Skin-effect
- Substrate losses





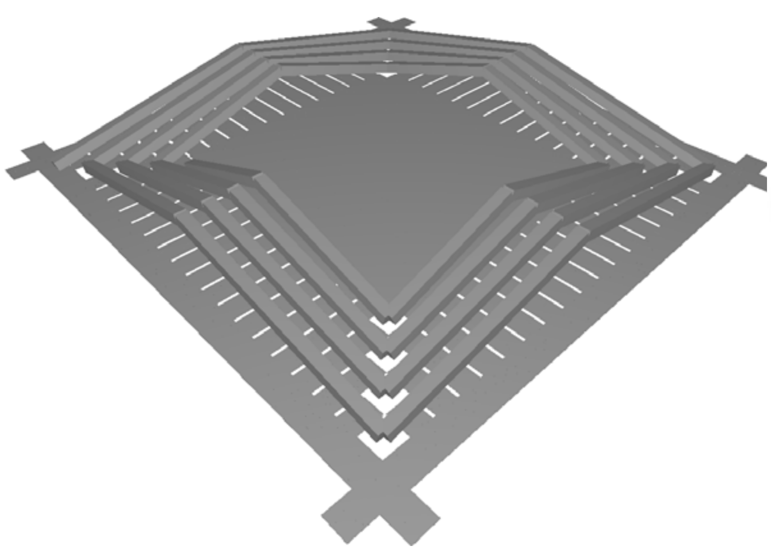


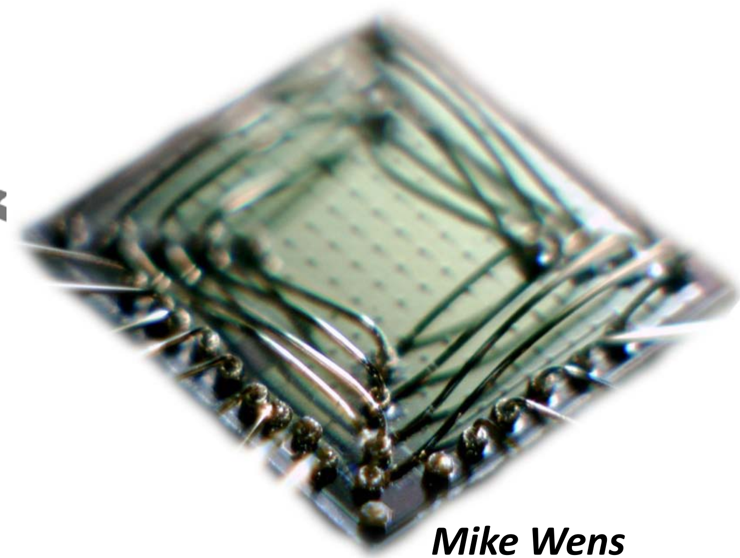
⟹ Round conductors & far from substrate/metal

Passives in CMOS

Bondwire inductors:

- Can be combined with C underneath (slots!)
- Low series resistance: ca. 50mΩ/nH @ 100MHz
- Far from substrate
- Good for single-phase & high voltage
- Cannot be scaled well: no multiphase





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Passives in CMOS

Metal-track inductors:

- Cannot be combined with C underneath
- High series resistance: ca. 250mΩ/nH @ 1GHz
- Close to substrate
- Good for multiphase & low voltage

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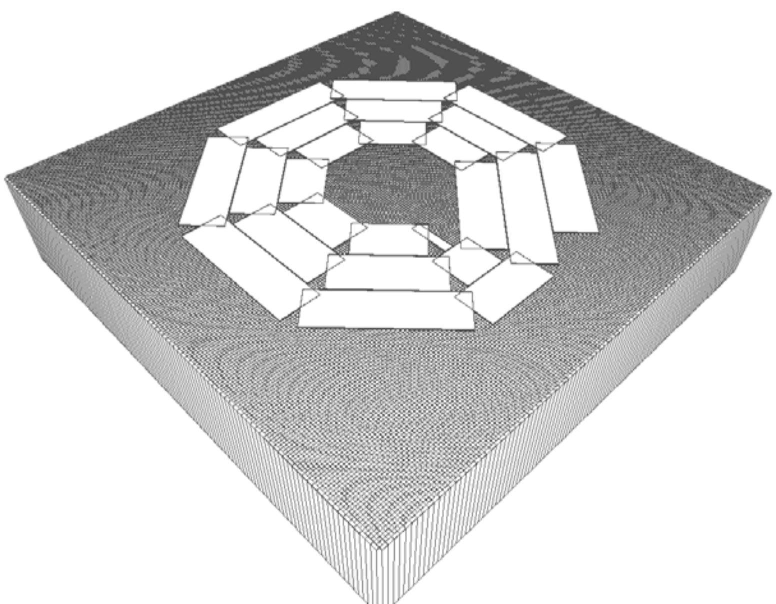
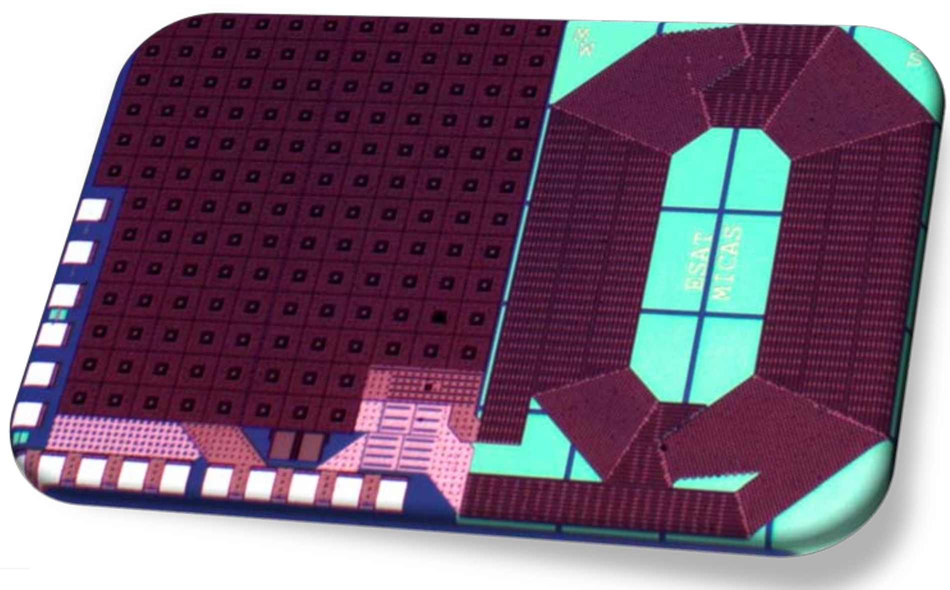


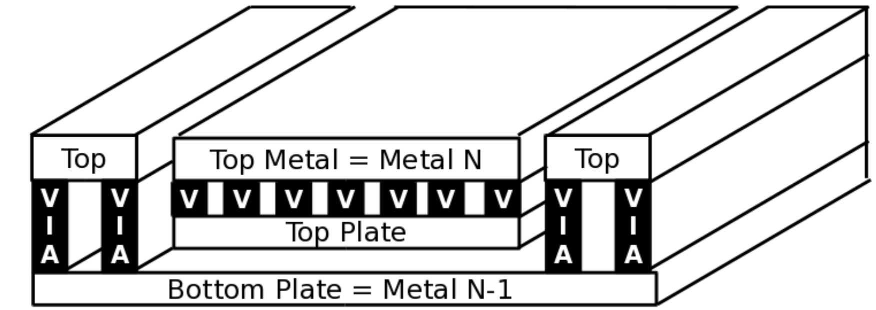


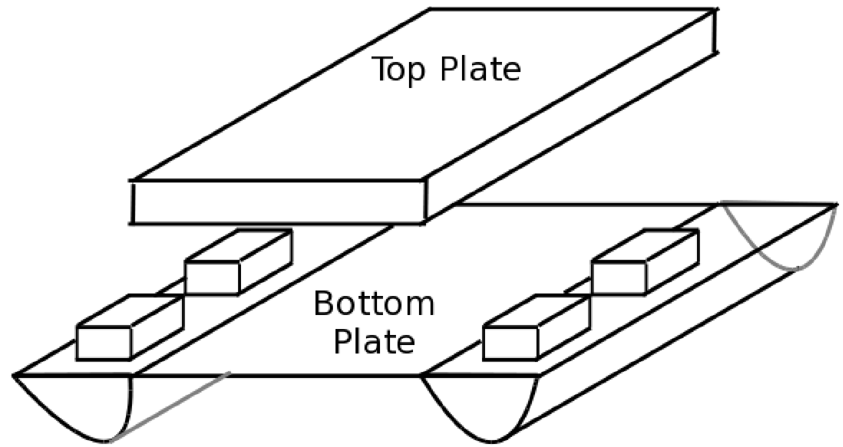
DC-DC in CMOS: Passives

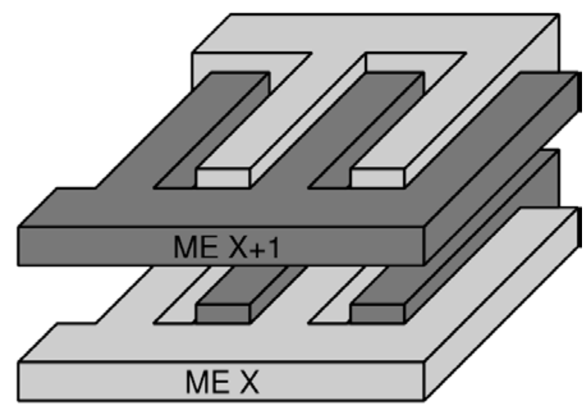
- Capacitors

Passives in CMOS

- Capacitors
  - MIM Capacitors
    - Low Density
    - High Quality
    - Voltage Independent Cap
  - MOS Capacitors
    - High Density
    - Improving with Scaling
    - Voltage Dependent Capacitance
      - Non Linear
  - MOM Capacitors
    - Low Density
    - High Quality
    - High voltage



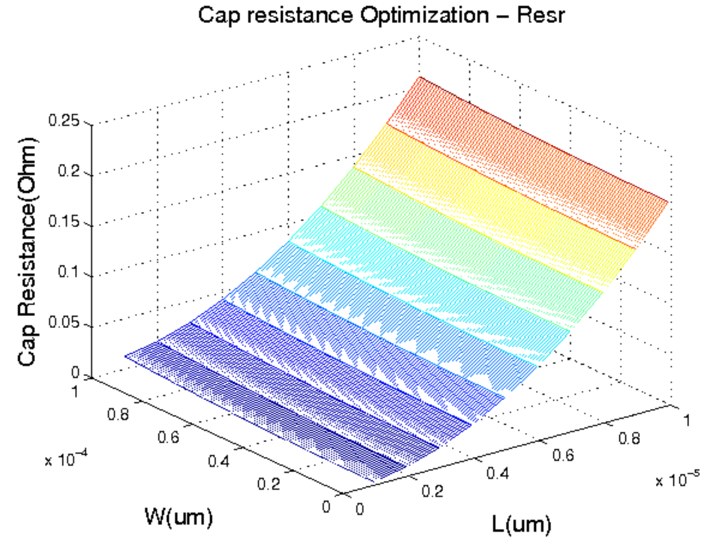


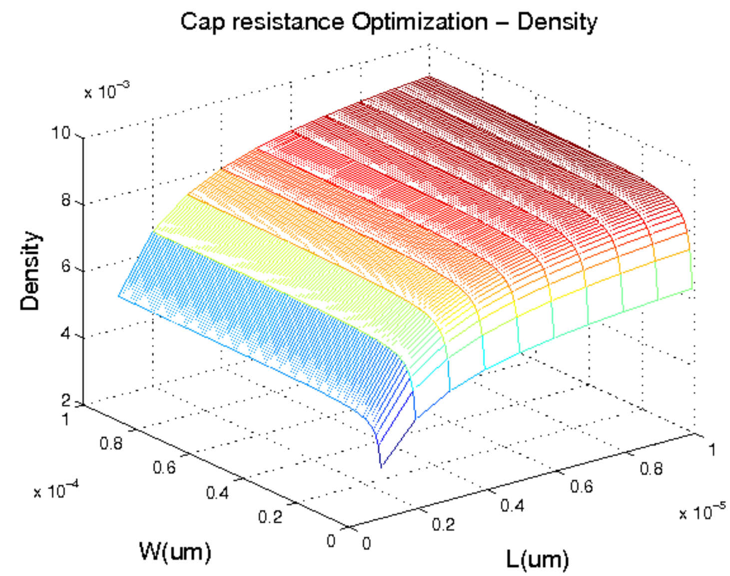


Passives in CMOS

- Capacitance Density
  - Type dependant
    - MOS-cap: ~10nF/mm²
    - MIM-Cap: ~2nF/mm²
    - MOM-Cap: ~0.5nF/mm²
  - Layout dependant
    - MIM-cap:
      - Poor Modeled
      - Little Layout freedom
    - MOS-cap
      - Poor Modeled
      - Lots of Layout freedom
      - Trade off

        Cap Density <> Resr



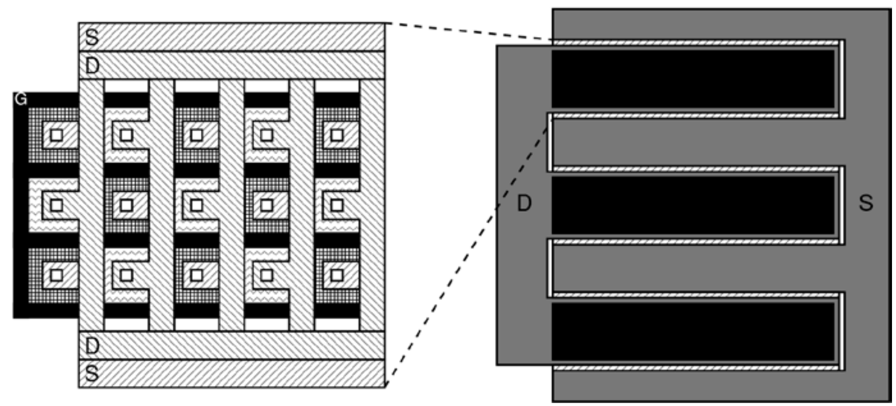


DC-DC in CMOS

- Actives

Actives in CMOS

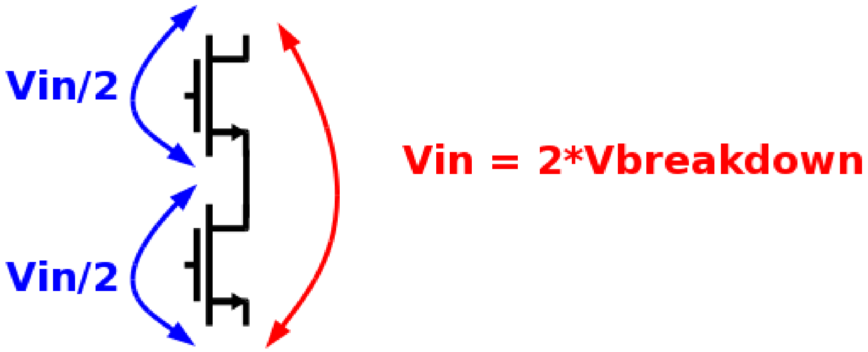
- Only CMOS switches
  - CMOS is good in switching at high frequencies
  - This is necessary since small amount of passives
  - Close Integration with control
  - Adapted waffle layout for low parasitics



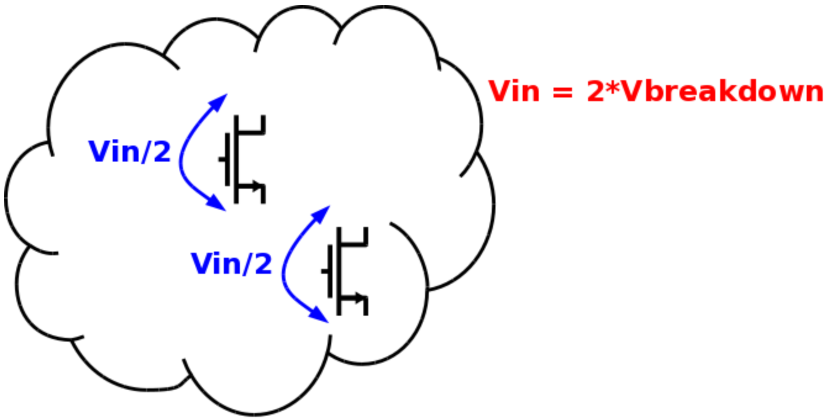
- But
  - Small breakdown voltage
    - Standard devices
      - 1-1.2V
      - Fast
    - IO devices
      - 2.5V-3.3V
      - Fast but not as fast as Standard Performance Devices
- **Solution:**
  - Use Switch Stacking
    or
    Voltage Domain Stacking

Actives in CMOS

- Switch Stacking
  - Put multiple switches in series to deal with higher voltages
    - Compensate for increase of R_{switch} -> Increase W
  - Hard for complex topologies and large # of switches in topology
  - Works perfect for Buck or Boost Cfr. Implementations

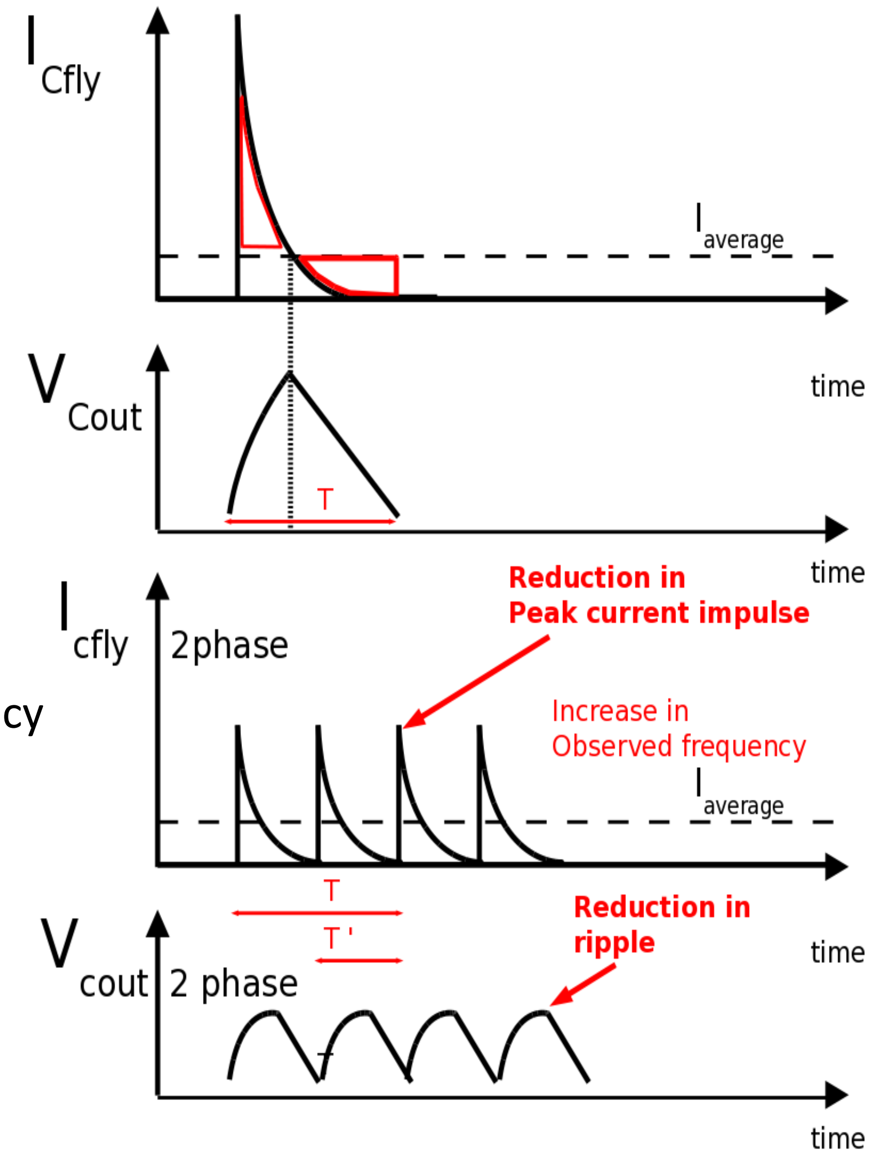


- Voltage Domain Stacking
  - Introduce multiple voltage domains
  - Make sure each switch in single domain
  - Take care of Start Up and transient behavior



Control

- Monolithic Integration enables
  - High Speed Control
  - Compact integrated solution
  - Extreme Multiphase
- But impedes
  - Current Measurement
  - Digital Control
    - 100MHz-1GHz switching frequency
    - DSP does not comply with this



Intermezzo: Efficiency Enhancement Factor (EEF)

DC-DC$_1$		DC-DC$_2$
$P_{out} = 1$ W $\quad k_{lin} = k_{SW} = 0.8$		$P_{out} = 1$ W $\quad k_{lin} = k_{SW} = 0.5$
$\eta_{lin} = 80~\%$ $\quad \eta_{SW} = 85~\%$ $\Longrightarrow \Delta\eta = \eta_{SW} - \eta_{lin} = 5~\%$ $P_{in\_lin} = 1.25$ W $\quad P_{in\_SW} = 1.18$ W $\Longrightarrow \Delta P_{in} = P_{in\_lin} - P_{in\_SW} = 0.07$ W $EEF = \left.\frac{\Delta P_{in}}{P_{in\_lin}}\right\vert_{k_{lin}=k_{SW}} = 5.6~\%$		$\eta_{lin} = 50~\%$ $\quad \eta_{SW} = 55~\%$ $\Longrightarrow \Delta\eta = \eta_{SW} - \eta_{lin} = 5~\%$ $P_{in\_lin} = 2$ W $\quad P_{in\_SW} = 1.82$ W $\Longrightarrow \Delta P_{in} = P_{in\_lin} - P_{in\_SW} = 0.18$ W $EEF = \left.\frac{\Delta P_{in}}{P_{in\_lin}}\right\vert_{k_{lin}=k_{SW}} = 9~\%$

$$\Longrightarrow \boxed{EEF = 1 - \left.\frac{\eta_{lin}}{\eta_{SW}}\right\vert_{k_{lin}=k_{SW}}}$$

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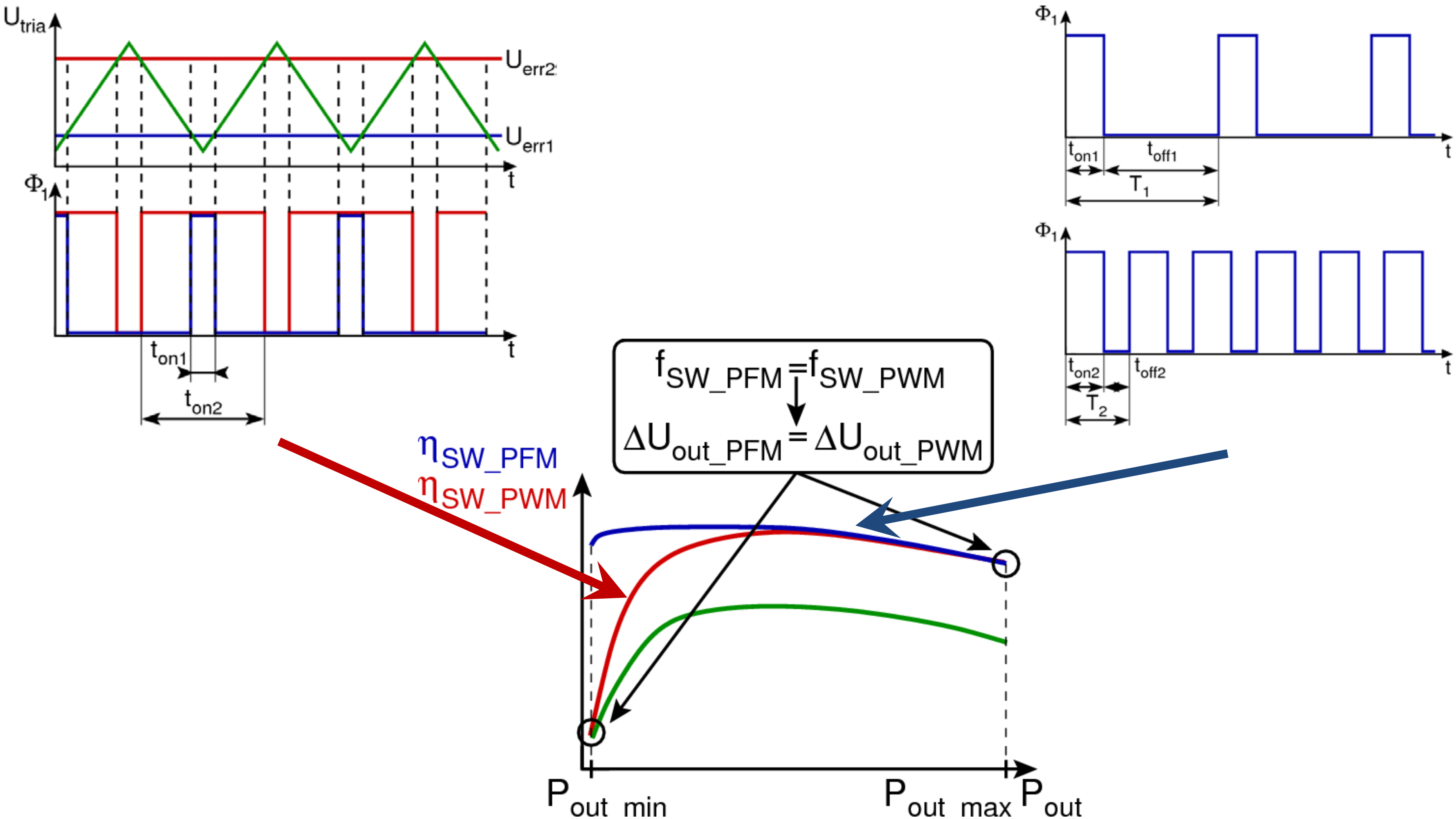
Inductive Converters: Control

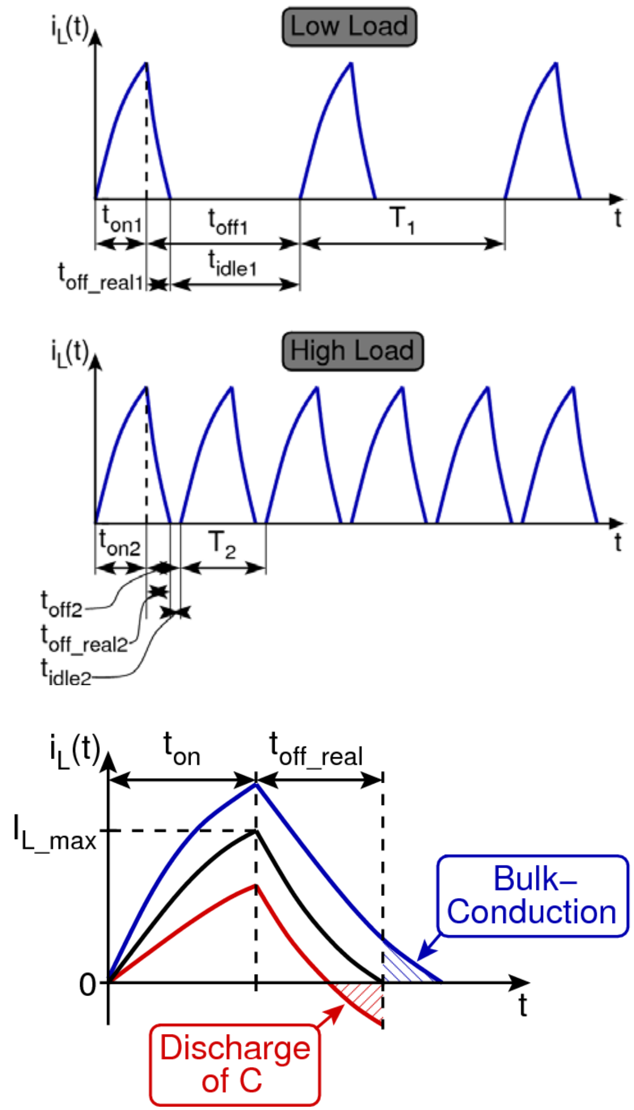
PWM vs PFM:



Inductive Converters: Control

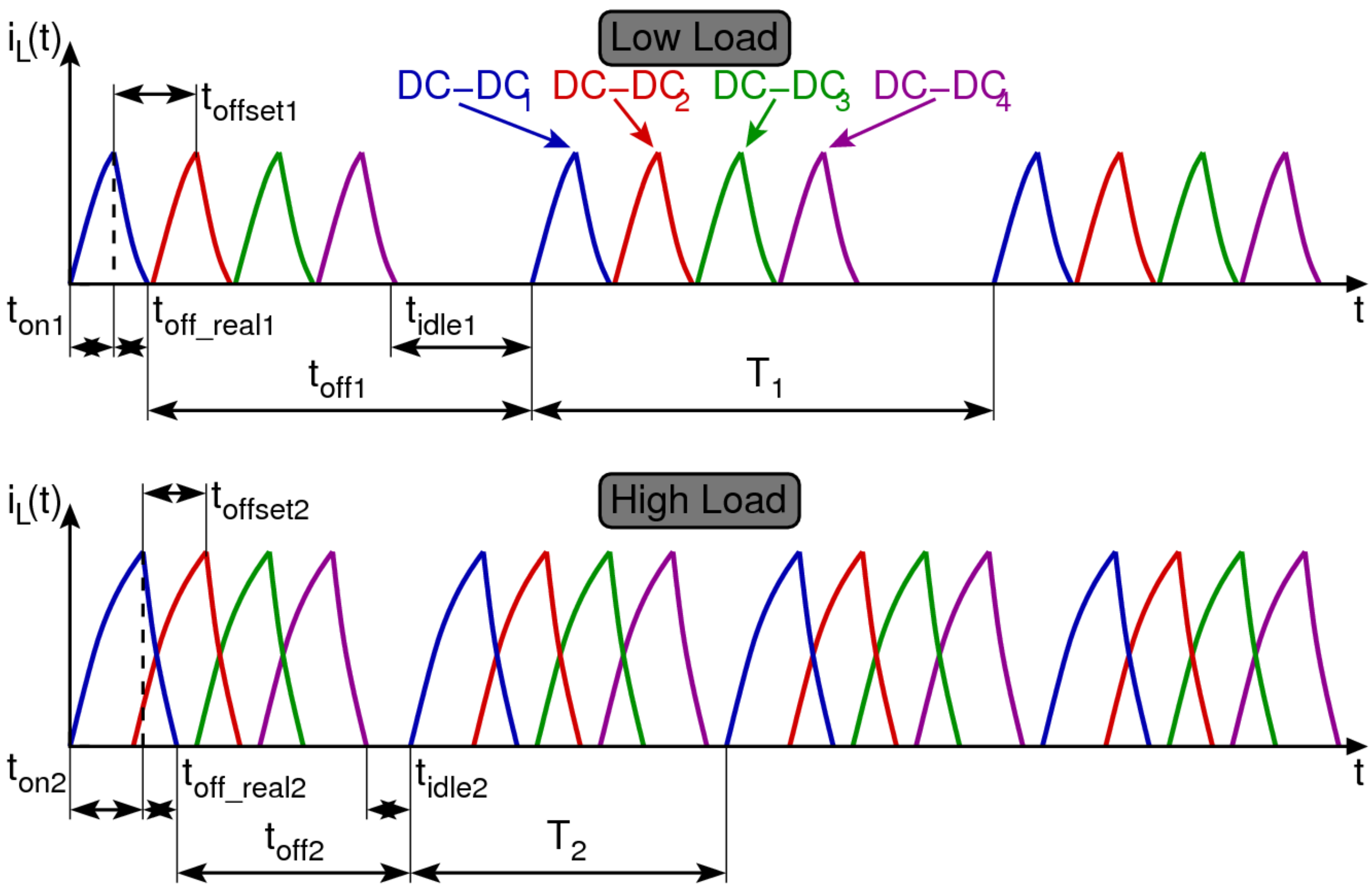
Constant On/Off-Time (COOT):

- Higher eff. vs PWM
- No current sensing
- Mostly digital
- Fast trasient response
- Fixed voltage ratio
- Load regulation dependant on the ripple



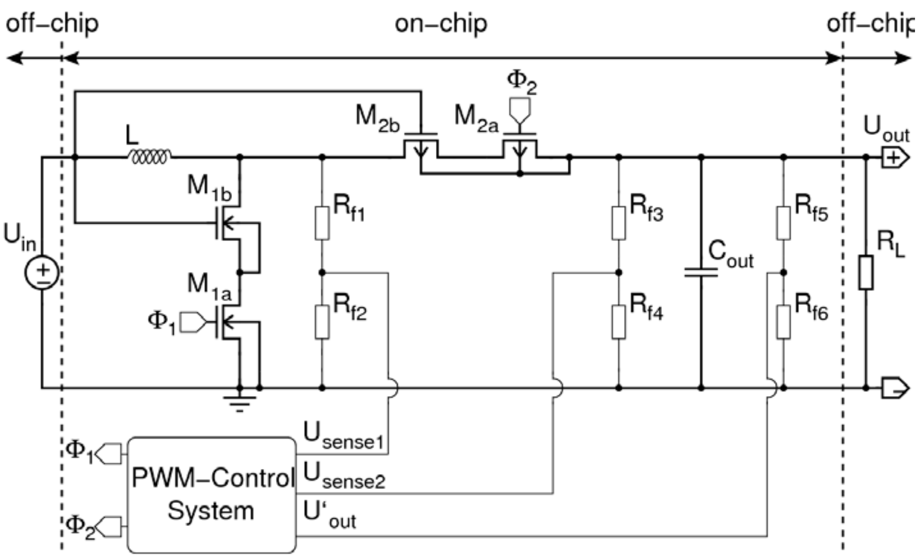
Inductive Converters: Control

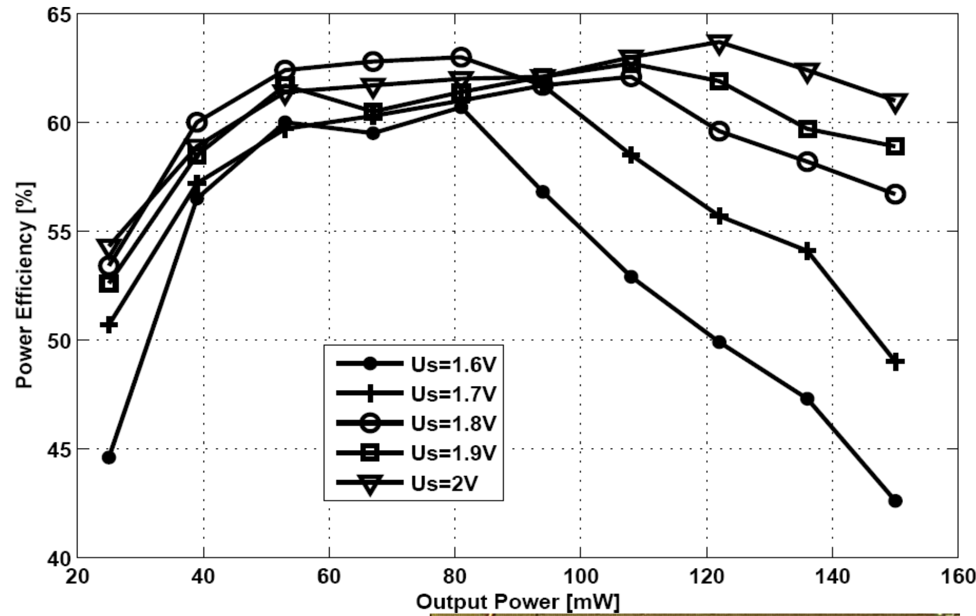
Semi-Constant On/Off-Time (SCOOT):



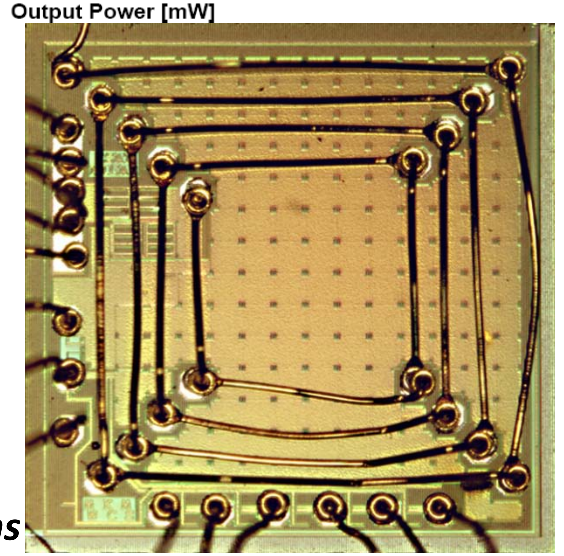
Inductive Converters

PWM example:





Input voltage range	1.6 V-2 V
Output voltage range	2.5 V-4 V
Output power range	25 mW-150 mW
Maximum power efficiency @ U_{out} =3.3 V	63 %
Maximum output ripple	200 mV
Maximum load variation	9 MHz
Switching frequency	100 MHz



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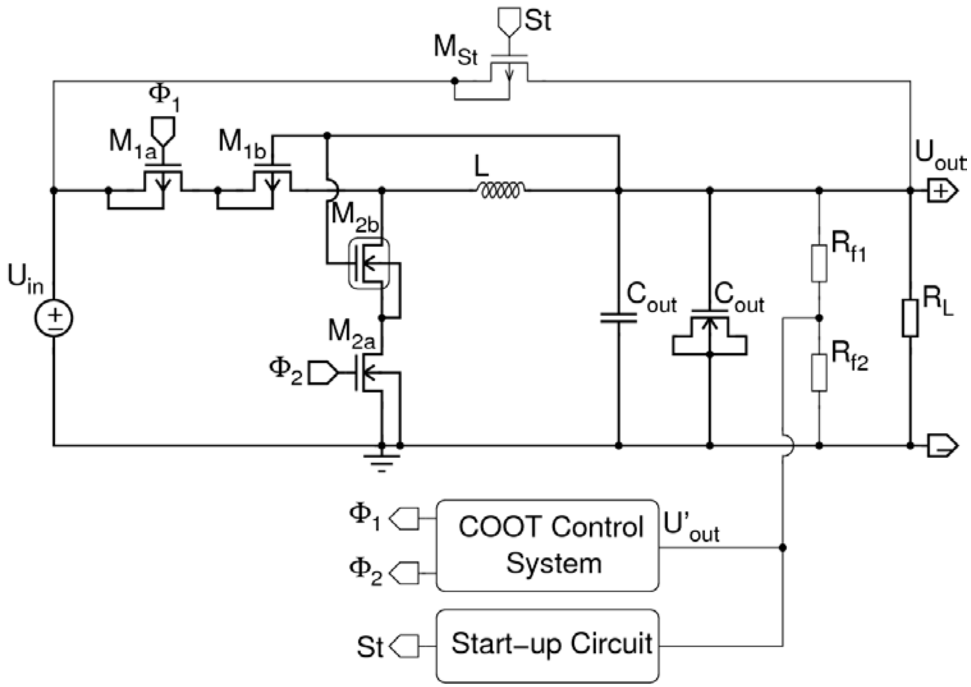
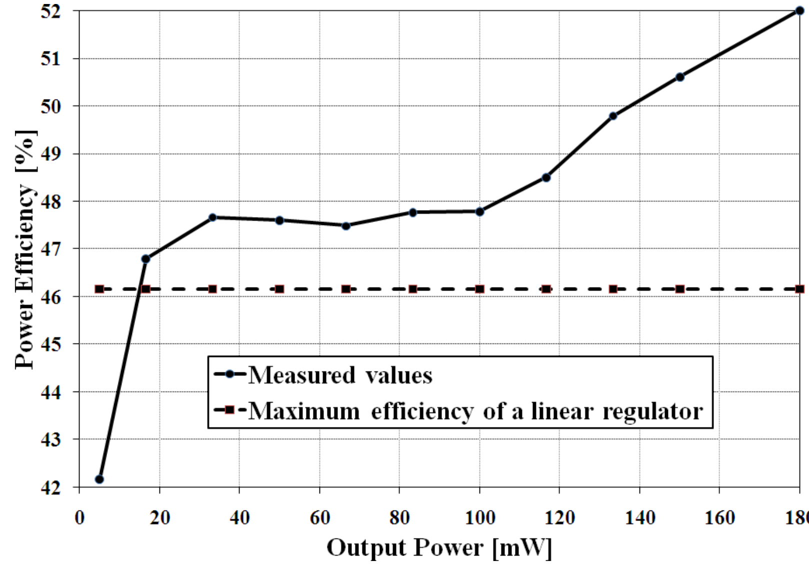
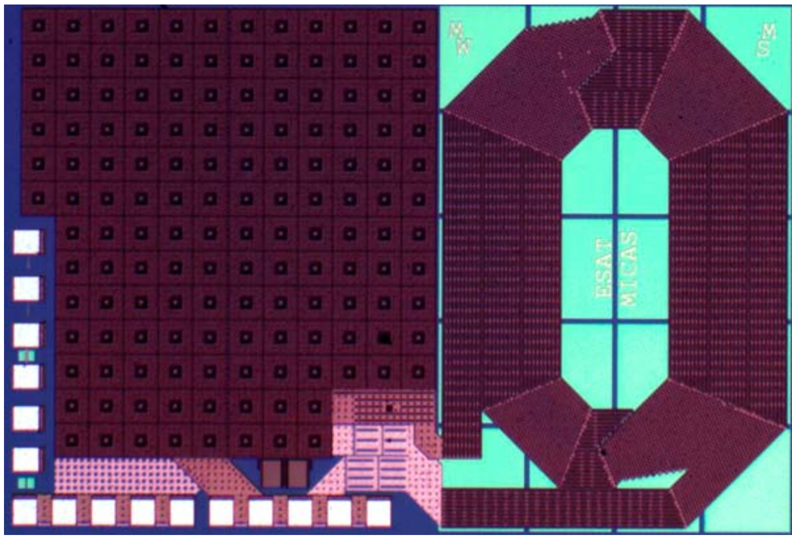
Inductive Converters

COOT example 1:





Input voltage range	2 V-2.6 V
Output voltage range	1.1 V-1.5 V
Output power range	0 mW-180 mW
Switching frequency range	30 Hz-300 MHz
Power efficiency @ U_{in} =2.6 V and U_{out} =1.2 V	52 %
Efficiency Enhancement Factor	12 %
Maximum output ripple @ P_{out} =0 mW	110 mV
Minimum output ripple @ P_{out} =180 mW	60 mV
Load regulation $\delta u_{out}/\delta i_{out}$	$-0.51\ \Omega$
Line regulation $\delta u_{out}/\delta u_{in}$	-0.083



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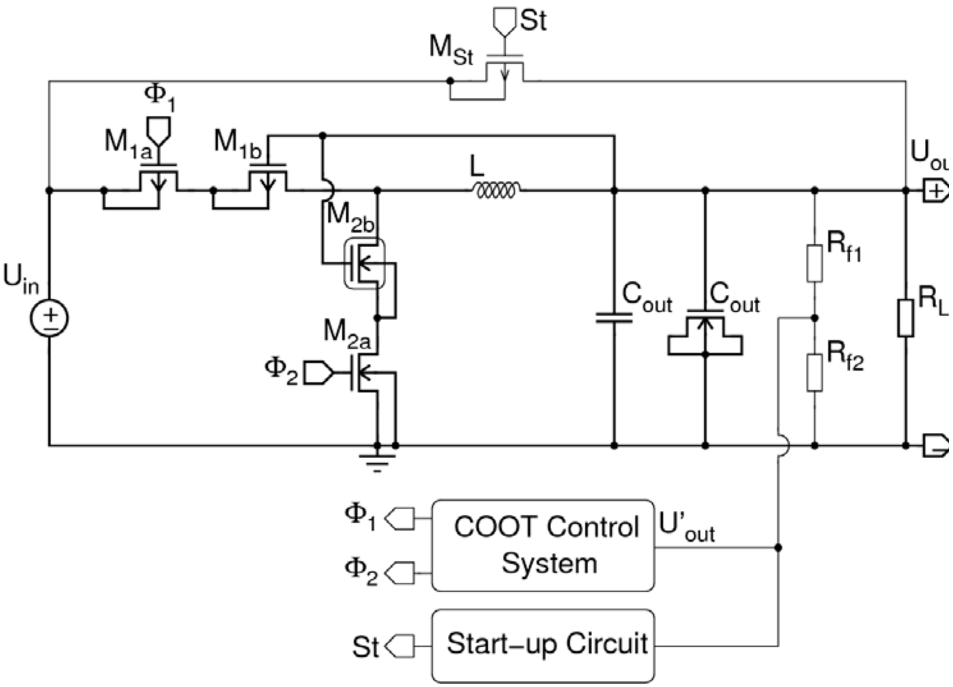
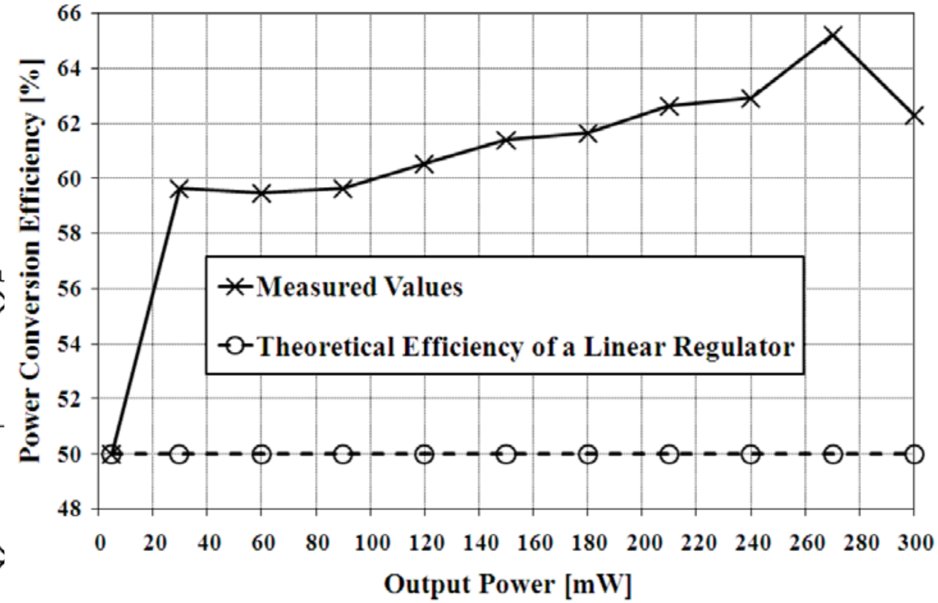
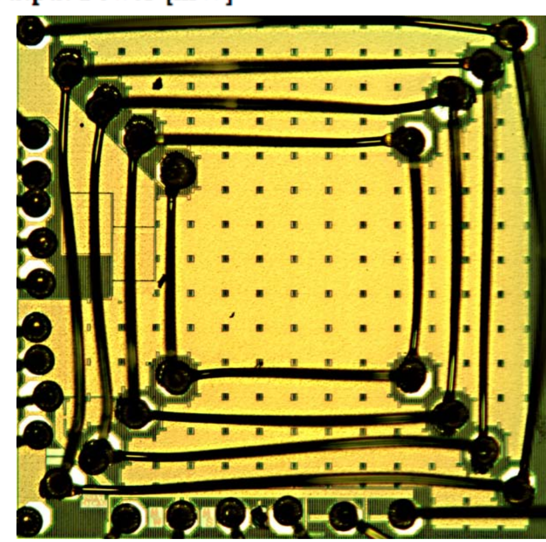
Inductive Converters

COOT example 2:





Input voltage range	3 V-4 V
Output voltage range	1.5 V-2.1 V
Output power range	0 mW-300 mW
Switching frequency range	20 Hz-140 MHz
Power efficiency @ U_{in} =3.6 V and U_{out} =1.8 V	65 %
Efficiency Enhancement Factor	23 %
Maximum output ripple @ P_{out} =0 mW	160 mV
Minimum output ripple @ P_{out} =300 mW	50 mV
Load regulation $\delta u_{out}/\delta i_{out}$	$-0.3\ \Omega$
Line regulation $\delta u_{out}/\delta u_{in}$	0.02



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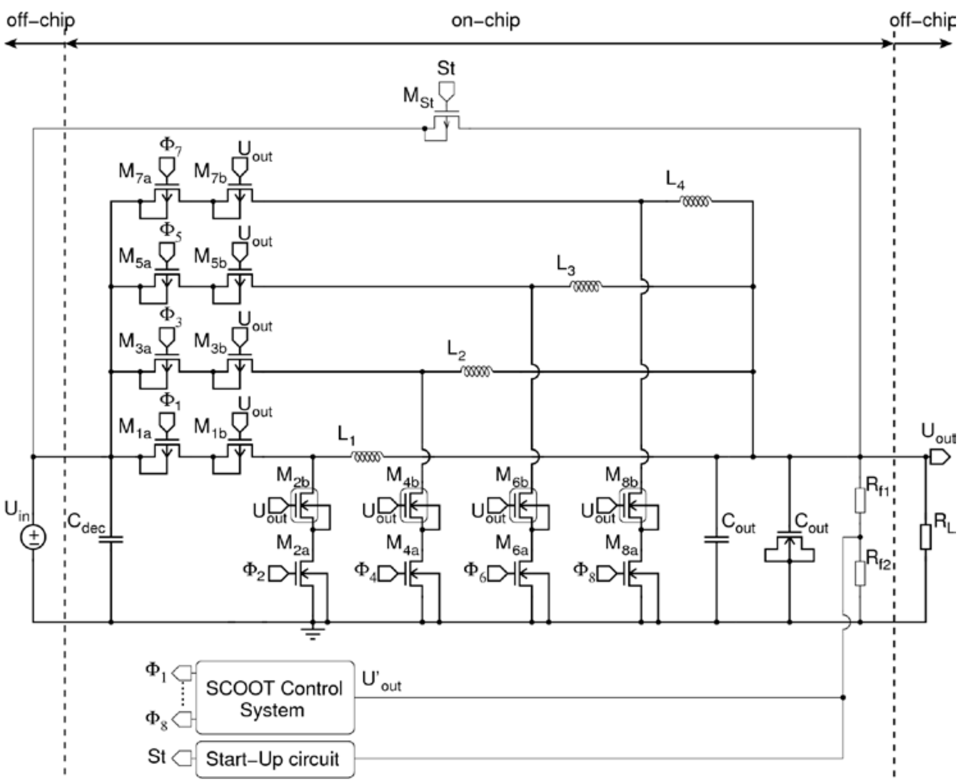
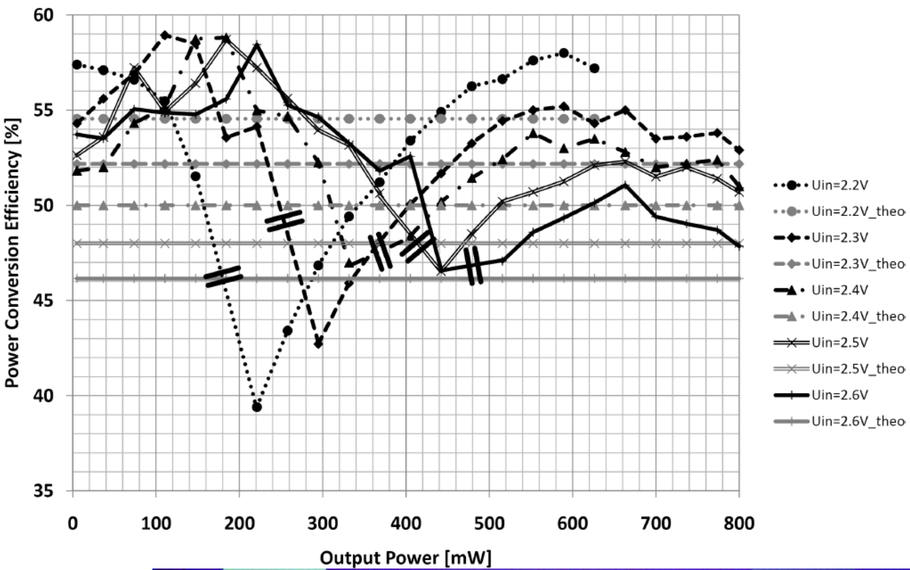
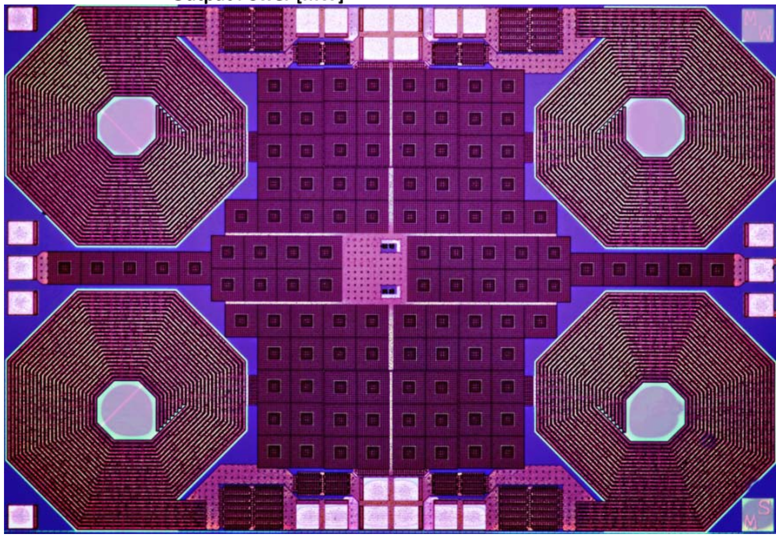
Inductive Converters

SCOOT example:







- **Output Power 800mW**
- **Efficiency Enhancement Factor +21%**
- **Power density 213mW/mm²**

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Published ECCE 2009 – San-José

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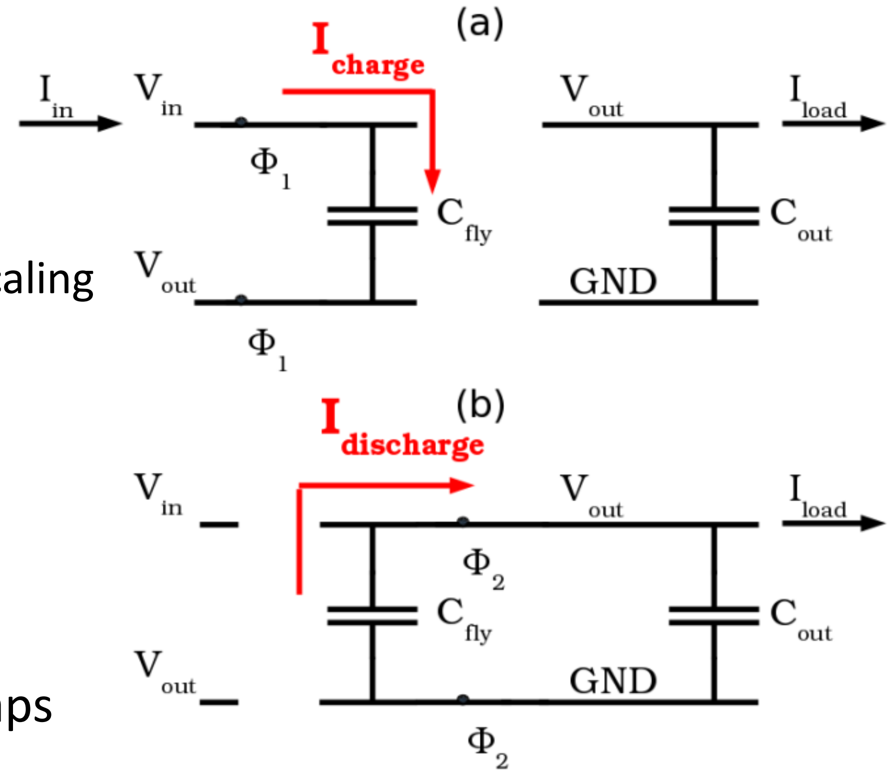
Capacitive Converters

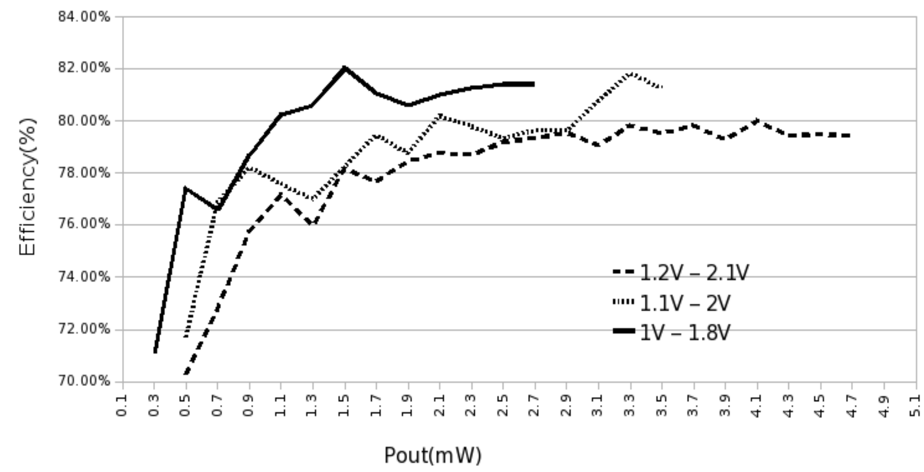
- Use nothing but
  - Solid state switches
  - Capacitors
    - Density and Quality increase by scaling

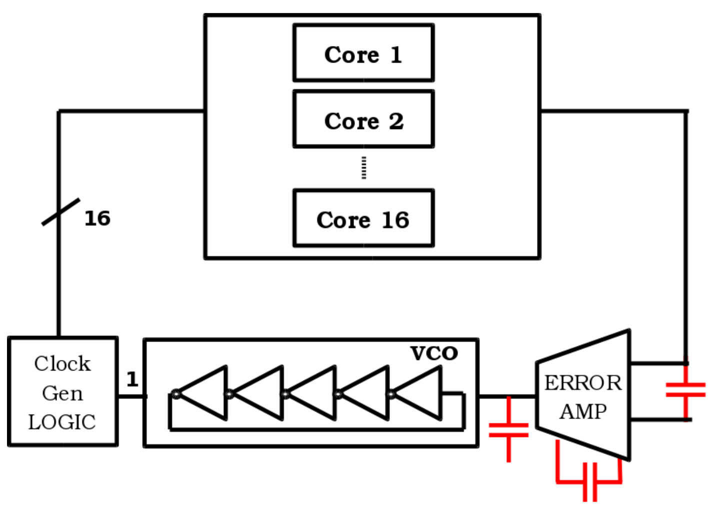
- 2-Phase operation
  - Topology corresponds with VCR
  - VCR:1/2 -> 1 cap || VCR:4/5 ->3 caps

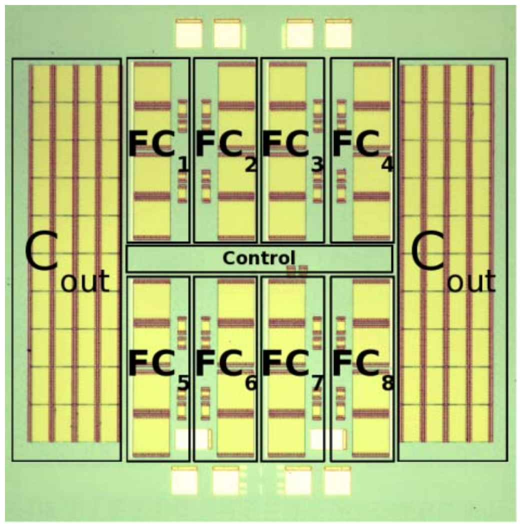


Capacitive Converters

- Up-Conversion
  - The voltage Doubler design
    - Multiphase – 16 phase
    - Analog Loop
    - Ripple < 0.5%
    - Efficiency up to 82%







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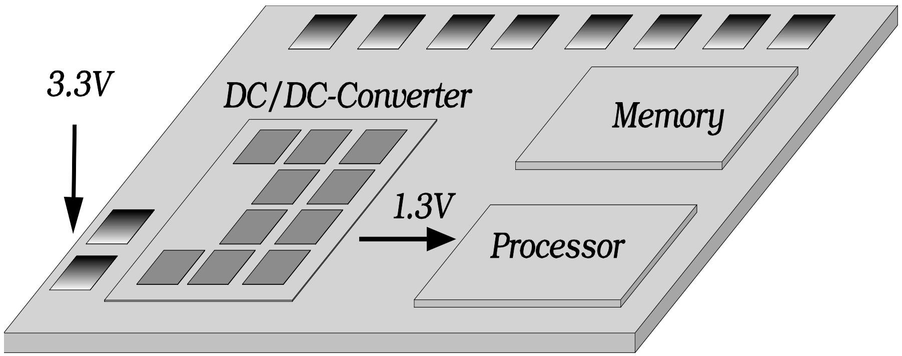
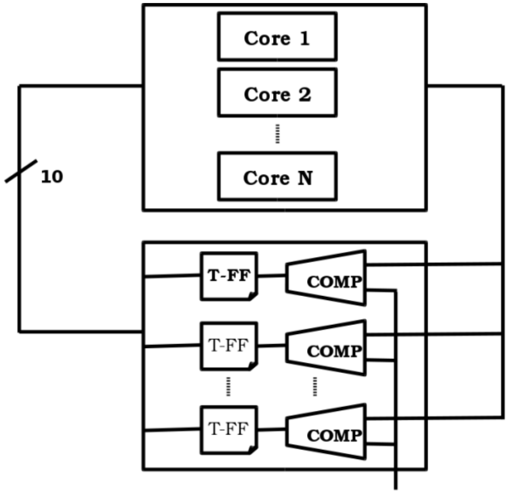
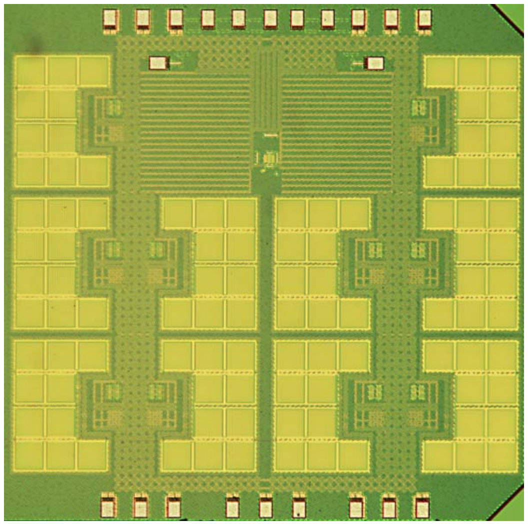
Capacitive Converters

- Down Conversion
  - Point Of Load Converter
    - 3.9V-3.05V Input
    - 1.52-1.3V Output
    - 150mW Max Pout
    - 77% Efficiency
  - Multiphase Hysteretic Control







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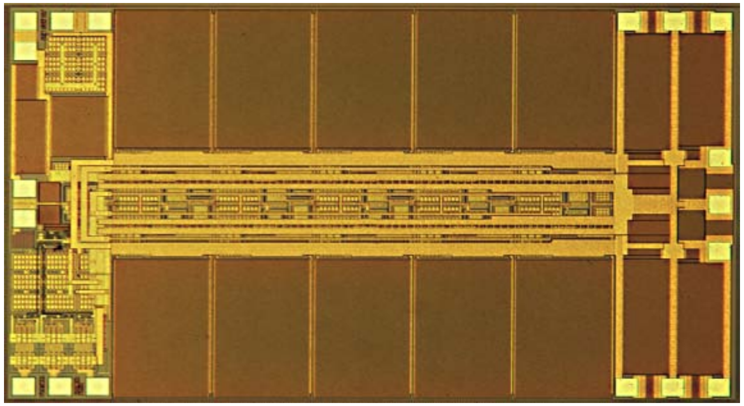
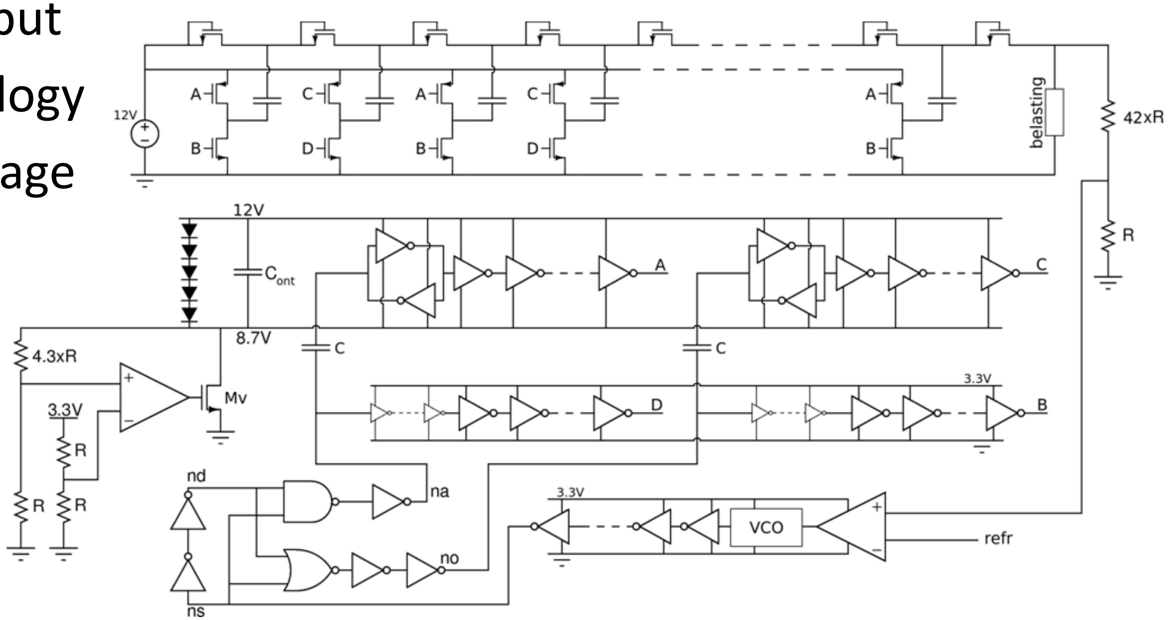
Capacitive Converters

- High Voltage Up-Conversion
  - The 10-stage High Voltage Dickson
  - 300mW
  - 70V output – 12V Input
  - High Voltage Technology
  - Efficiency 86% per stage





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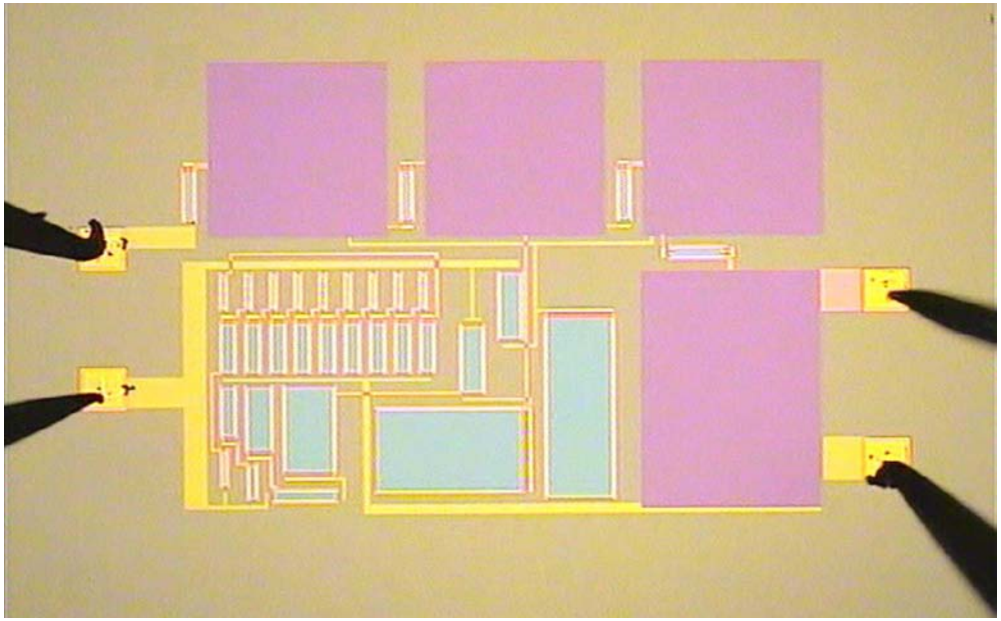
Capacitive Converters

- Organic DC-DC
  - No CMOS but cheap
  - 'Plastic'-technology
  - Only PMOS
  - Cap-type Converter
    - 3-stage Dickson
  - 18V Input
    60V Output



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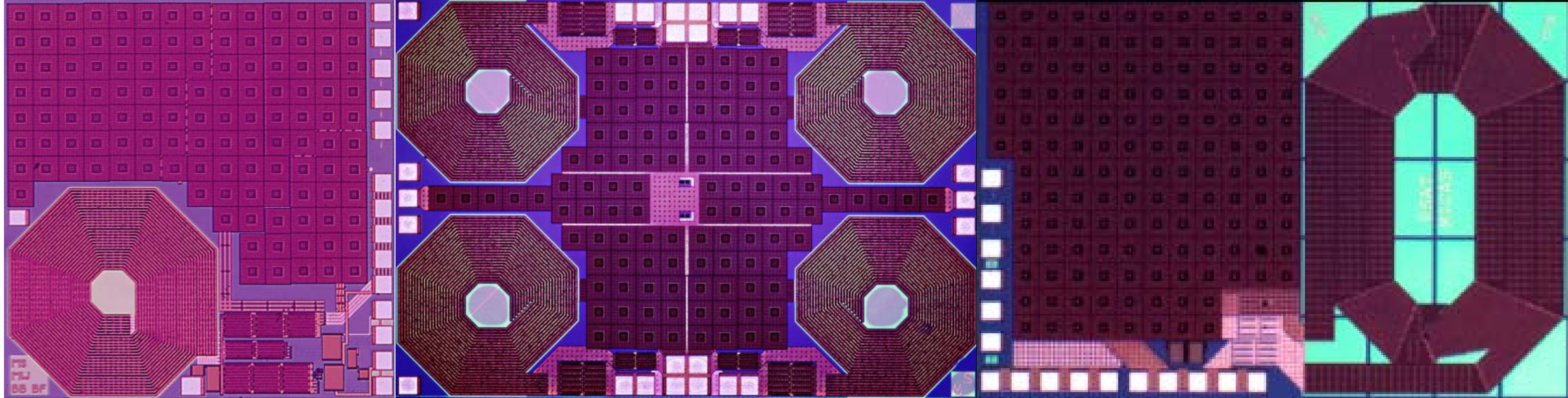
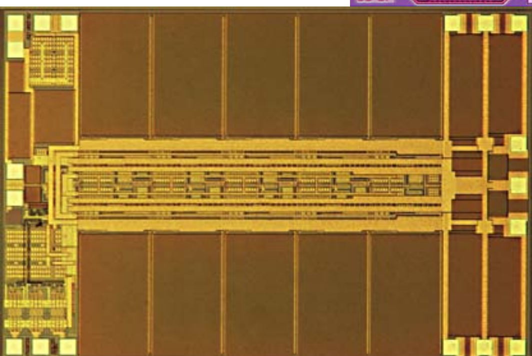
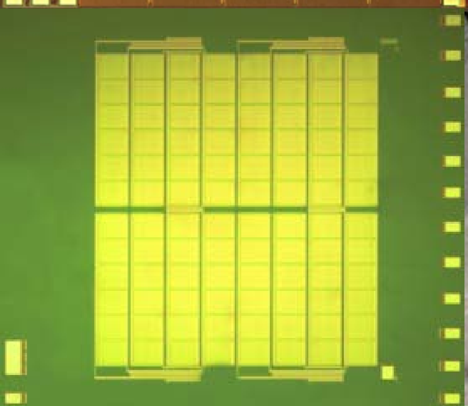
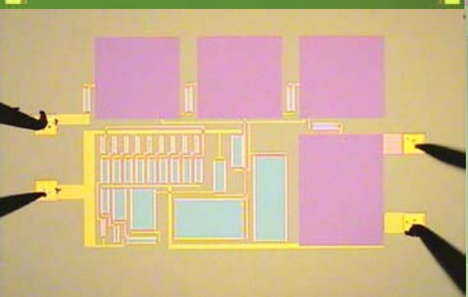
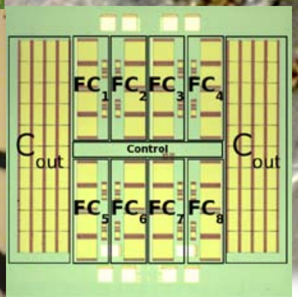
Overview

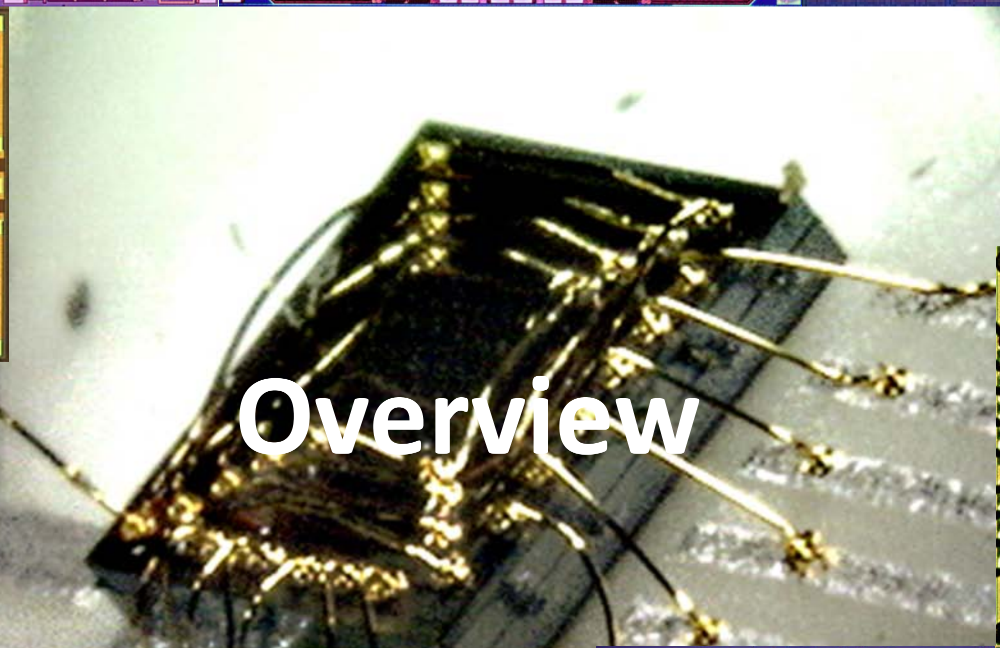


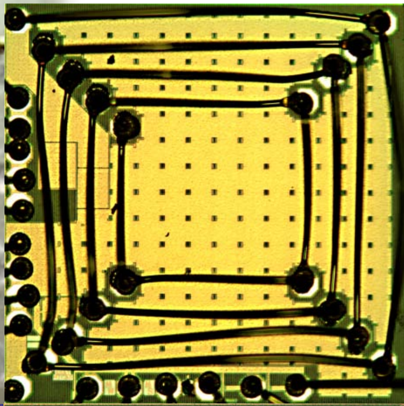


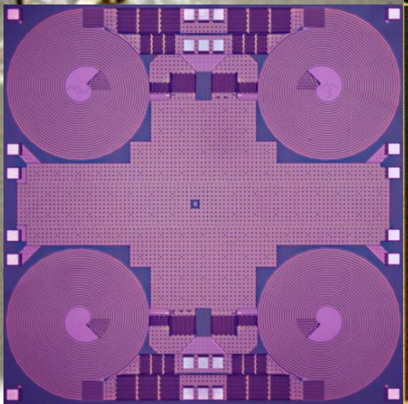


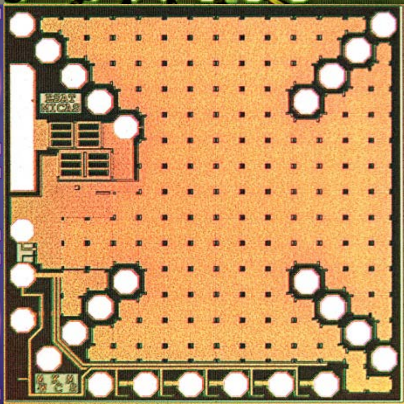












Conclusion

- POWER-CMOS is the logic evolution of RF-CMOS
  - Continue the development of high performing fully-integrated DC-DC converters to set a new milestone in integrated circuits
- Cost-effective Bulk CMOS is able to deliver attractive DC-DC converter specifications
  - Go multiphase
  - Go digital control
- Inductive converters: main issue is inductor quality (and ESR)
- Capacitive converters: quest for higher densities (attention to ESR)
- Use EEF as benchmark to validate performance compared to linear regulator

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  - Tom Van Breussegem
  - Hagen Marien
  - Piet Callemeyn
- **More info**

www.esat.kuleuven.be/micas/powercluster